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(54) IC card memory arrangement for recording and reproducing audio and/or video data concurrently and s parately

(57) In an arrangement for selectively recording and playing back audio and video data using an IC card memory as a recording medium, the card has an index region in which card attribution and miscellaneous intrinsic card data are recorded, a mode code region in which codes identifying the data type of respective chapters are recorded, a chapter pointer region in which the address where each chapter starts is recorded and a data region in which the actual data of each chapter is stored. The method includes the steps of selecting a predetermined chapter and recording mode (i.e. video or audio), recording the code of the selected mode, recording the starting address of the chapter in a pointer address if a recording key input is detected, recording a mode monitoring code in the starting address and recording the video and/or audio data in subsequent addresses, and recording data indicating the end of the chapter in the last address when data input is completed. The mode codes allow the generation of latch-enabling signals for gating audio and video signals input to D/A converters or output from A/D converters (Figs 3-6). Therefore, the apparatus and method according to the present invention can record and play back audio and/or video data concurrently or separately.

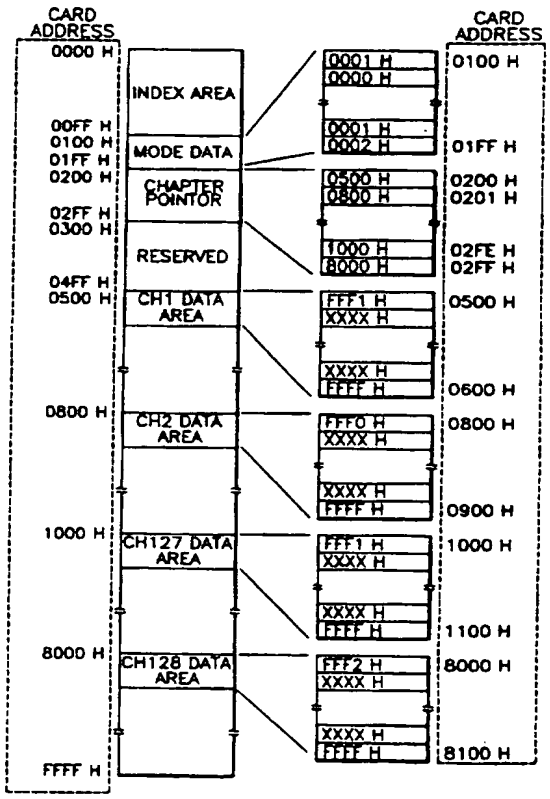

FIG. 2

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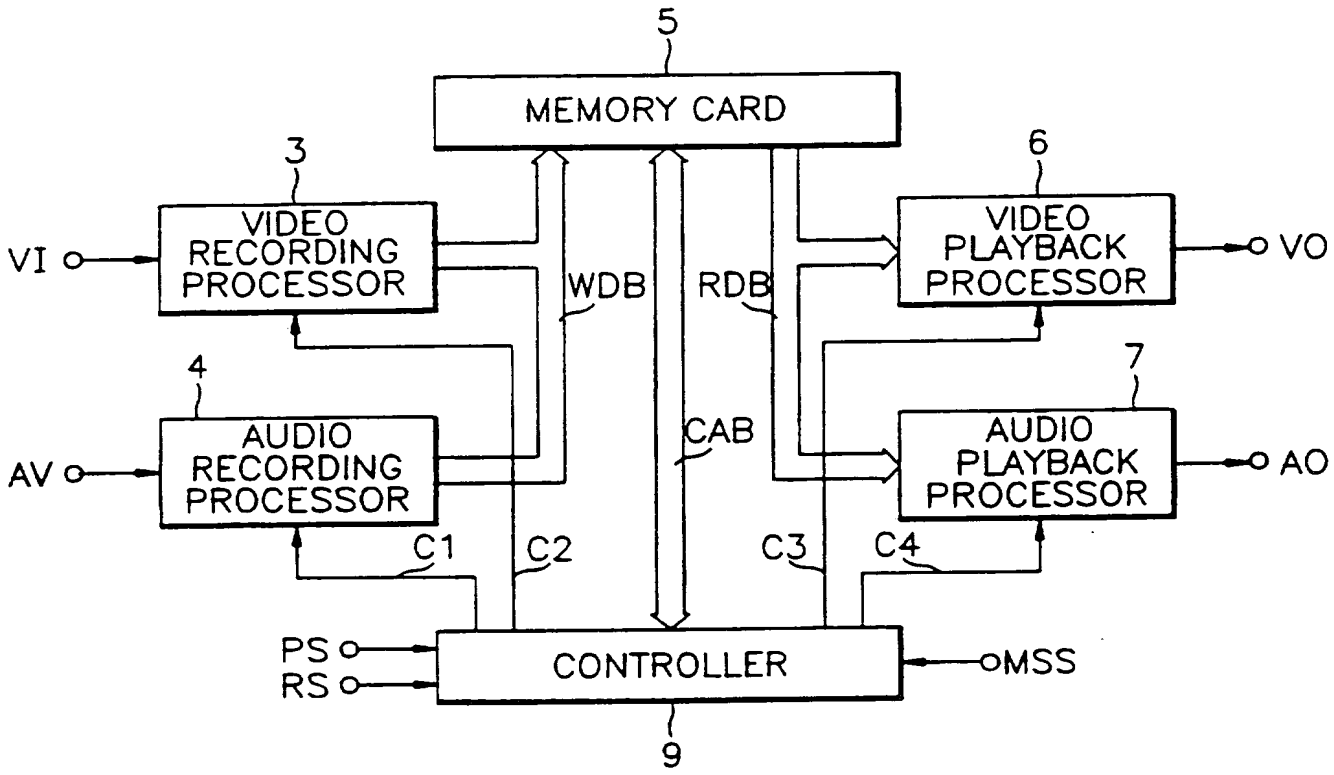

(PRIOR ART)

FIG. 1

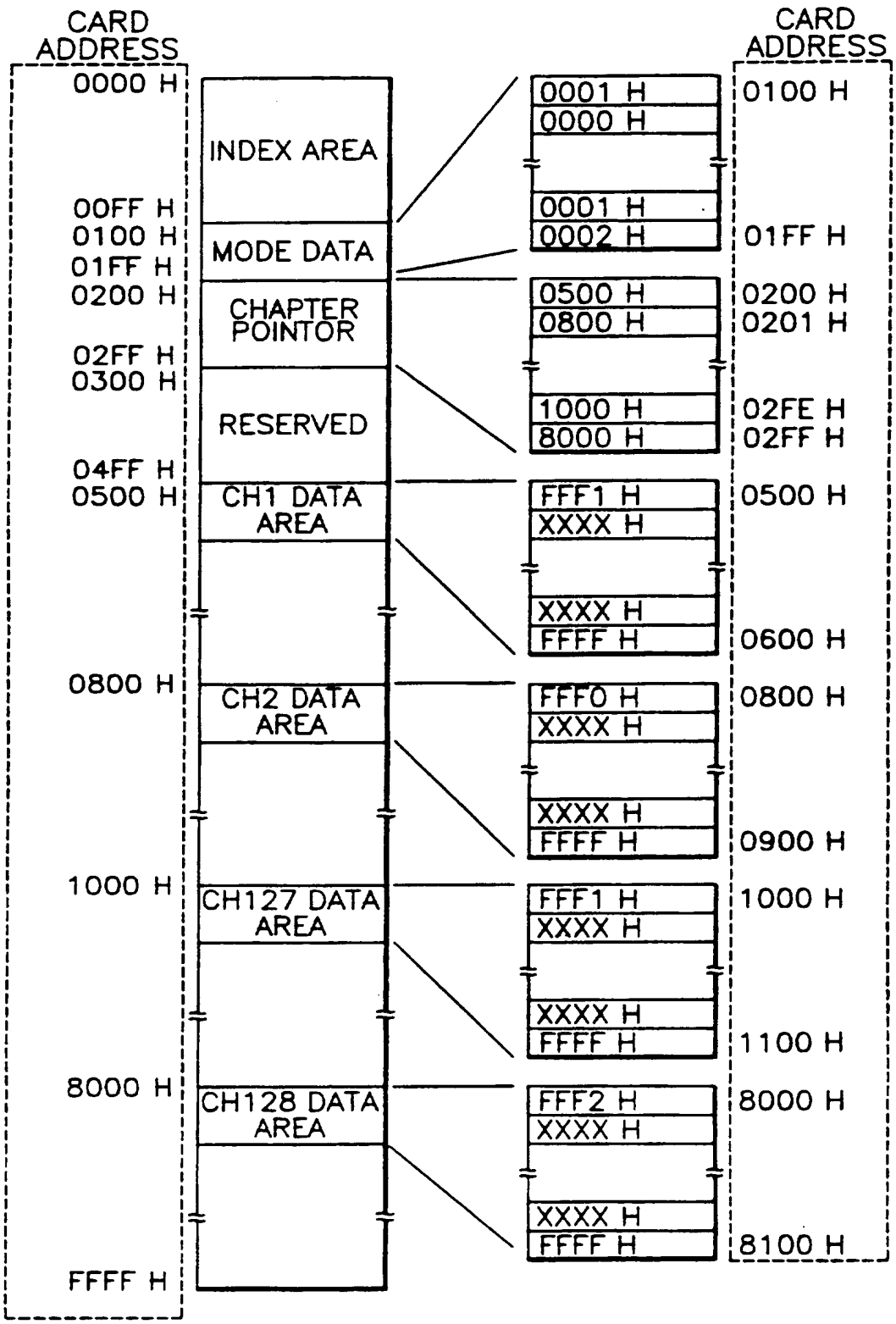

FIG. 2

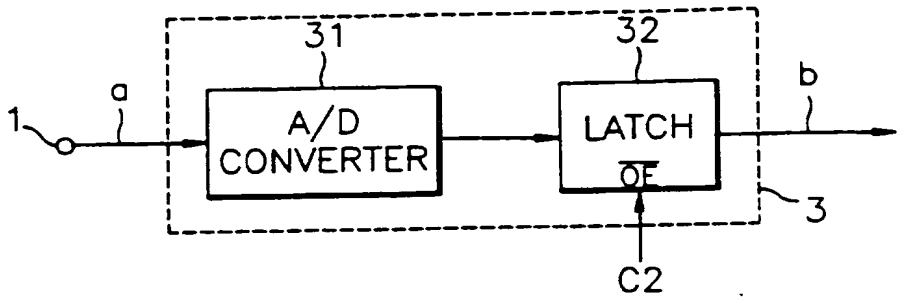

FIG. 3

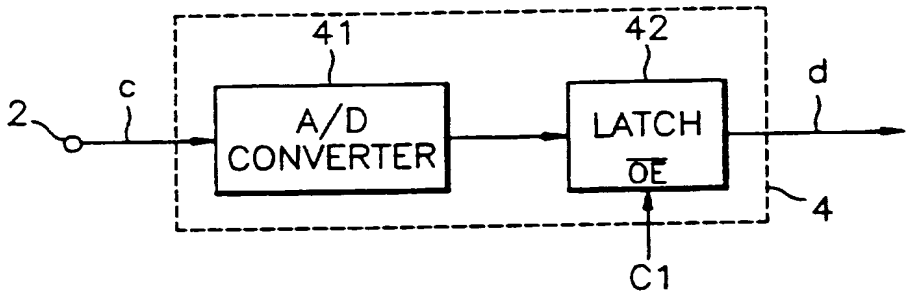

FIG. 4

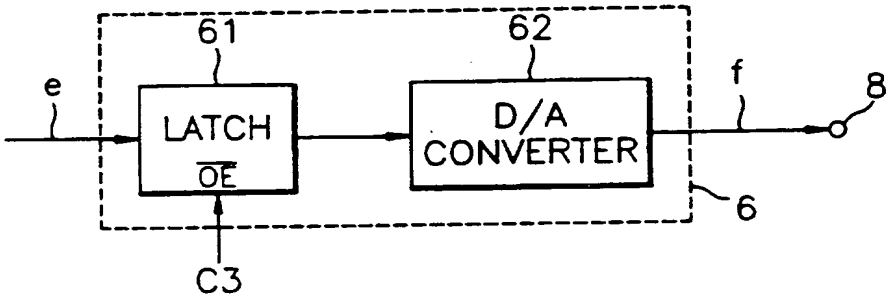

FIG. 5

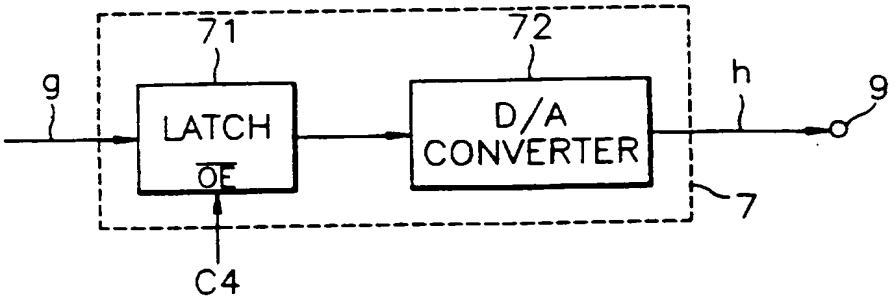

FIG. 6

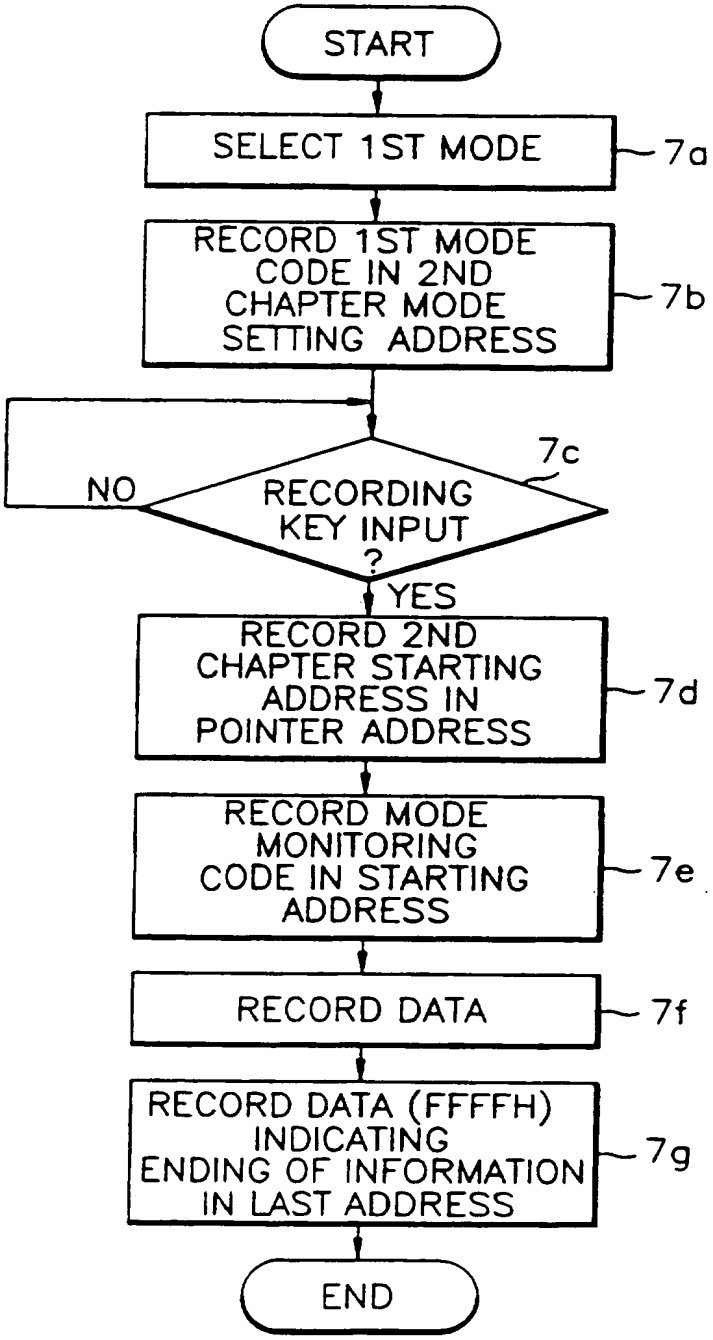

FIG. 7

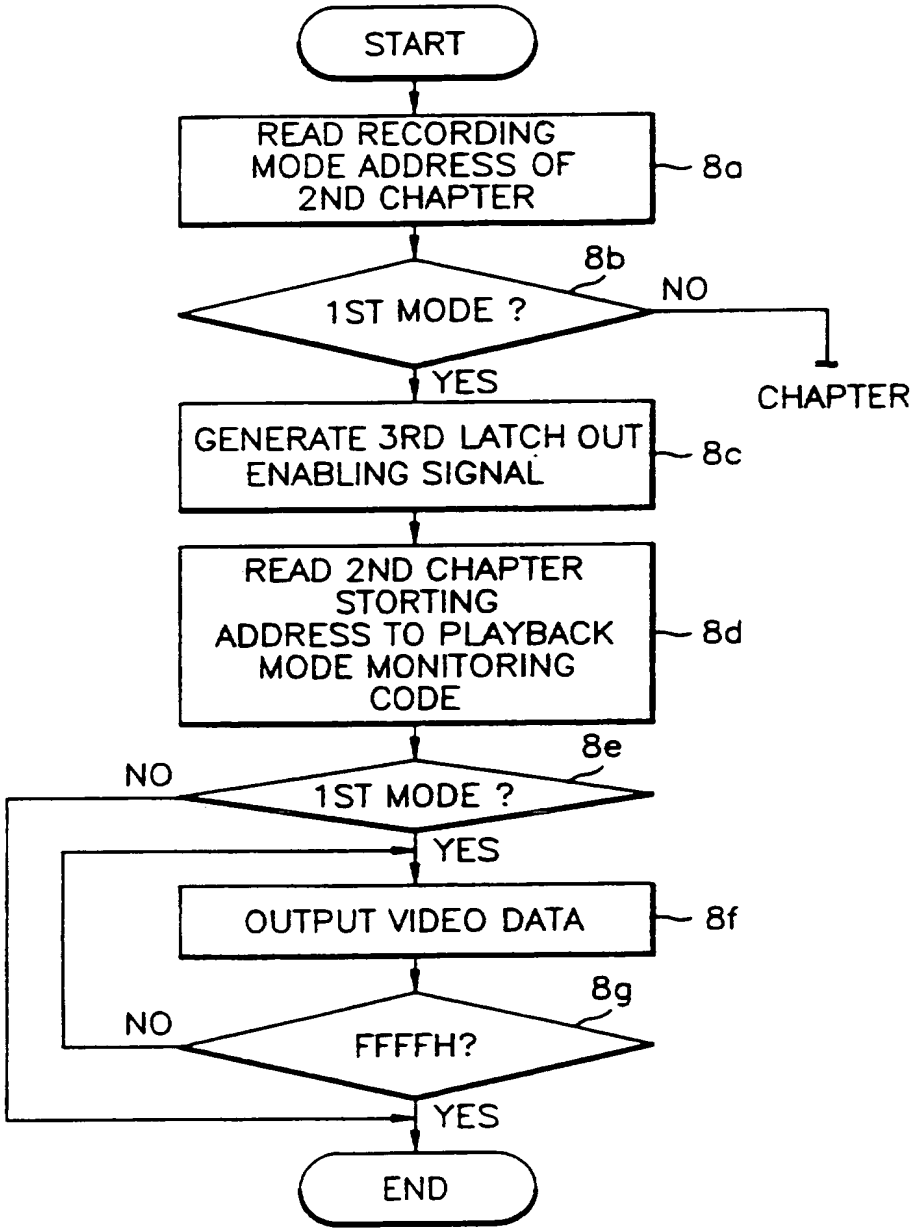

FIG. 8

IC CARD MEMORY FOR RECORDING AND REPRODUCING AUDIO AND/OR VIDEO DATA CONCURRENTLY AND SEPARATELY AND CONTROLLING METHOD THEREOF

The present invention relates to an apparatus and method for recording and playing back audio and video data using an IC card memory as a recording medium, and more particularly, to an apparatus and method for recording and playing back audio and/or video data concurrently or separately.

Figure 1 is a block diagram of a general apparatus for recording and playing back audio and video using an IC card memory as a recording medium, in which analog video and audio signals VI and AV are input to video and audio recording processors 3 and 4, respectively and the processing result is recorded in an IC card memory 5. At this time, all controlling operations are performed such that a controller 9 sets control lines C1 through C4 depending on input conditions of a playback switch PS, a recording switch RS, and a mode switch MSS. If playback switch PS is turned on, controller 9 reads out the content recorded in IC card memory 5, and applies the video or audio data selected according to the mode to video or audio playback processor 6 or 7.

The conventional audio and video recording apparatus having the aforementioned configuration should concurrently record video and audio data, but cannot record only audio data nor still picture data.

Th refore, it is an aim of preferred embodiments of the present invention to provide an IC card memory which can record and reproduce audio and/or vid o data

concurrently and separately, and a controlling method thereof.

According to a first aspect of the invention, there is provided an IC card memory comprising:

an index region in which card attribution and miscellaneous intrinsic card data are recorded;

a mode code region in which data for setting recording or playback type of a chapter is recorded;

a chapter pointer in which the address where each chapter starts is recorded in a memory region; and

a data region in which the actual data of each chapter is stored.

According to a second aspect of the present invention, there is provided a method for recording audio and video data using an IC card memory having a mode code region with data for setting a recording or playback type of a chapter being recorded therein as a recording medium, the method comprising the steps of: selecting a predetermined chapter and a recording mode; recording a code of the selected mode in the mode set address of the selected chapter; recording a starting address of the chapter in a pointer address if a recording key input is detected; recording a mode monitoring code in the starting address and recording data corresponding to the subsequent addr sses; and recording data indicating the end of the chapter to the last address if data input is compl ted.

According to a third asp ct of the pres nt invention, there is provided a method for r cording audio and video

data using an IC card memory having a mode code region with data for setting a recording or playback type of a chapter being recorded therein as a recording medium, the method comprising the steps of: selecting a predetermined chapter; reading a recording mode address of the selected chapter to determine a mode; generating a video, an audio or a composite latch out enabling signal in accordance with the determined mode; and outputting a video, an audio or a composite data in response to the latch out enabling signal.

Preferably, the method further comprises the steps of reading a mode monitoring code in a starting address of said chapter to reconfirm the mode, and proceeding to a next step only when the reconfirmed mode coincides with the determined mode.

According to a fourth aspect of the invention, there is provided a method for recording audio and video data, using an IC card, the method comprising:

(i) selecting a recording mode for the selection of audio, video or combined audio/video recording;

(ii) storing mode data on the IC card, the mode data corresponding to the recording mode selected in step (i);

(iii) recording either audio data, video data or combined audio/video data accordingly, on said IC card; and

(iv) storing an address point r for designating the storage address at which said recording is commenced.

The method may further comprise any feature or combination of features from the accompanying description, claims, abstract or drawings.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a general block diagram of an apparatus for recording and playing back audio and video using an IC card memory as a recording medium;

Figure 2 is a schematic diagram of a data map within an IC card memory according to an embodiment of the present invention;

Figure 3 is a detailed schematic diagram of a video recording processor shown in Figure 1;

Figure 4 is a detailed schematic diagram of an audio recording processor shown in Figure 1;

Figure 5 is a detailed schematic diagram of a video playback processor shown in Figure 1;

Figure 6 is a detailed schematic diagram of an audio playback processor shown in Figure 1;

Figure 7 is a flowchart showing the process of recording data in a memory card according to embodiments of the present invention; and

Figure 8 is a flowchart showing the process of playing back data from a memory card according to embodiments of the present invention.

It should be noted that like reference numerals and letters are used to designate like or equivalent elements, throughout the drawings. Also, various specific things such as components of a detailed circuit shown in the following explanation are only supplied for the sake of whole understanding of the present invention. However, it is obvious to one having ordinary skill in the art that the present invention can be embodied without such specific things. In explaining the present invention, the detailed explanation of the related well-known functions or components, which may make the essence of the present invention vague will be omitted.

In this embodiment, a mode code for prescribing the characteristics of input data is generated. In detail, a first mode for recording only video data is 0000H. A second mode for recording only audio data is 0001H. A third mode for recording both video and audio data is 0002H. In this manner, if a mode is set by a mode switch MSS, a controller 9 generates such a mode code and records the same in an IC card memory 5.

Figure 2 is a schematic diagram of a data map within an IC card memory 5 according to an embodiment of the present invention. First, in view of an overall memory, addresses corresponding 0000H to FFFFH are set. However, such a setting may be varied depending on the attribution of the card. Here, the region ranging from the initial 0000H to 00FFH is an index region, in which information data such as a card size, maker, manufacturing year, recording time or recording date is recorded. The index

region contains attribution of a card and miscellaneous information, which is not practically relevant to the audio or video data. Next, the region ranging from 0100H to 01FFH is a region where mode codes (an essential part of the present invention) are recorded. In this embodiment, since the number of total chapters are limited to 128, the mode codes corresponding to the respective chapters are also limited to 128. Here, the chapter which is a recorded data unit represents the data of one cycle of executed recording operation until it stops. The mode code of a first chapter is recorded in an address 100 and the mode code of a second chapter is recorded in an address 101. In this manner, if a chapter is mapped in an address and is increased, mode codes of 128 chapters are recorded in the last address 1FF. The next addresses 0200H through 02FFH are pointer addresses corresponding to the respective chapters, from which the addresses of the respective chapters starts in the memory region. A pointer address code of a first chapter is recorded in an address 200, and a pointer address code of a second chapter is recorded in an address 201. In this manner, if a chapter is mapped in an address and is increased, pointer address codes of 128 chapters are recorded in the last address 2FF. The next addresses 300 through 4FF correspond to a reserve region, and is supplied for a user's optional use. The actual audio and video data are recorded from an address 500. In this embodiment, the first chapter starting address data included in the pointer address 200 of the first chapter is 500.

Figure 3 is a detailed schematic diagram of a video r cording processor 3 shown in Figure 1, in which reference letter a represents an analog video signal, which is convert d into a digital vid o signal by an analog-to-digital (A/D) converter 31. Next, the digital

video signal is input to a latch 32. A signal which enables latch 32 is a second out enabling control signal C2 output from a controller 9. If the second out enabling control signal C2 is low, the digital video signal is input to an IC card memory 5 through a bus *b*. If the second out enabling control signal C2 is high, latch 32 does not generate a digital video signal. Thus, there is no more input for IC card memory 5.

Figure 4 is a detailed schematic diagram of an audio recording processor 4 shown in Figure 1, in which reference letter *c* represents an analog audio signal, which is converted into a digital audio signal by an A/D converter 41. Next, the digital audio signal is input to a latch 42. A signal which enables latch 42 is a first out enabling control signal C1 output from controller 9. If the first out enabling control signal C1 is low, the digital audio signal is input to IC card memory 5 through a bus *b*. If the second out enabling control signal C2 is high, latch 42 does not generate a digital audio signal. Thus, there is no more input for IC card memory 5.

Figure 5 is a detailed schematic diagram of a video playback processor shown in Figure 1, in which reference letter *e* represents a digital video signal, which is input to a latch 61. A signal which enables latch 61 is a third out enabling control signal C3 output from controller 9. If the third out enabling control signal C3 is low, the digital video signal is converted into an analog video signal by a digital-to-analog (D/A) converter 62. If the third out enabling control signal C3 is high, the digital video signal does not input to D/A converter 62. Thus, there is no more reproduced signal.

Figure 6 is a detailed schematic diagram of an audio playback processor 7 shown in Figure 1, in which reference letter *g* represents a digital audio signal, which is input to a latch 71. A signal which enables latch 71 is a fourth out enabling control signal C4 output from controller 9. If the fourth out enabling control signal C4 is low, the digital audio signal is converted into an analog audio signal by a D/A converter 72. If the fourth out enabling control signal C4 is high, the digital audio signal does not input to D/A converter 72. Thus, there is no more reproduced signal.

Figure 7 is a flowchart showing the process of recording data in a memory card according to embodiments of the present invention. First, a chapter to be recorded is checked and a mode switch MSS is adjusted to set a mode (step 7a). In this embodiment, it is assumed that a first mode and a second chapter are selected. In this manner, if the first mode and the second chapter are selected, controller 9 records 0000H in the mode code region of the second chapter, i.e., address 0101 (step 7b). Thereafter, if it is detected that a recording key is input (step 7c), a starting address of a memory where the data of the second chapter is to be recorded is recorded in the chapter pointer (step 7d). If the first chapter is recorded from address 500 to 7FF, controller 9 recognizes that the starting address of the second chapter is address 800, and writes 800 in the pointer address 201 corresponding to the second chapter. Right after the recording in the pointer is completed, the recording of video data starts. In other words, the second latch out enabling signal C2 is generated. Also, the actual data is recorded in IC card memory 5. At this time, th first mode cod FFF0 is again written in the first address wh re th actual data is recorded, i.e., address 800, which is a

monitoring code for monitoring whether the code set by the mode code is the same as the data of the actual data recorded region (step 7e). The mode monitoring code functions to record data as the first mode of FFF0 before recording video data, in provision for the case that the mode codes positioned from the address 200 to the address 2FF are erased. Here, FFF1 is given as the second mode, and FFF2 is given as the third mode. In this manner, the monitoring code is recorded in the first address where the actual data is recorded, and the actual data is recorded from the second address, i.e., address 801. From this time, input data are sequentially recorded until data input stops. Then, data FFFF is inserted in the last address of the corresponding chapter so as to recognize that the chapter is used up. Then, the recording for the second chapter is terminated. (steps 7f and 7g).

Figure 8 is a flowchart showing the process of playing back data from a memory card according to the present invention, which is for the case that the data recorded onto the second chapter is read out. First, controller 9 designates the second chapter, and the mode code of the second chapter is first checked. Controller 9 searches the mode code data region of the second chapter to grasp the code (steps 8a and 8b). In this embodiment, it is assumed that the first mode is selected. The first mode code will be proved to be 0000H. Therefore, controller 9 outputs the third out enabling control signal C3 in low state to turn latch 61 on and outputs the other control signals C1, C2 and C4 in high state to turn latches 32, 42 and 71 off (step 8c). Thereafter, the second chapter pointer address is read out to interpret the address wh re the second chapter starts. In this embodiment, since th address where the second chapter starts is address 800, the content stored in th address

800 of IC card memory 5 is read out. At this time, the read data is a mode monitoring code (step 8d). The mode monitoring code is interpret and checked whether it is FFF0 by controller 9. If the data is FFF0, that is, if it is checked whether the mode set by the mode code is the same as the data of the actual data recorded region, and if they are the same, the data is read out so that the data is transmitted to video playback processor 6 shown in Figure 1. The transmitted data are converted into a video signal through a predetermined playback process to then be output (step 8f). If the data are consecutively read to reach FFFFH, it is determined to be an ending position by controller 9 and all playback operations are terminated. If the mode monitoring code is not data corresponding to the first mode, the information (message) indicating that the data is not reproducible should be notified to a user.

The recording and playback for modes of another chapters also operate in the same principle as described above.

As described above, the apparatus and method according to the present invention can record and play back audio and/or video data concurrently or separately. In other words, in the present invention, separate video and audio recording regions are not necessary, but the video and/or audio data can be recorded freely any time.

Although the present invention has been described and illustrated in detail, it may be variously modified within the spirit and scope of the present invention. Thus, the scope of the pres nt invention should not be limited to the above-described embodiment but should be defined by th appended claims and equivalents.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. An IC card memory comprising:

an index region in which card attribution and miscellaneous intrinsic card data are recorded;

a mode code region in which data for setting recording or playback type of a chapter is recorded;

a chapter pointer in which the address where each chapter starts is recorded in a memory region; and

a data region in which the actual data of each chapter is stored.

2. A method for recording audio and video data using an IC card memory having a mode code region having data for setting a recording or playback type of a chapter recorded therein as a recording medium, said method comprising the steps of:

selecting a predetermined chapter and recording mode;

recording a code of said selected mode in the mode set address of said selected chapter;

recording a starting address of said chapter in a pointer address if a recording key input is detected;

recording a mode monitoring code in said starting address and recording data corresponding to the subsequent addresses; and

recording data indicating the end of said chapter to the last address if data input is completed.

3. A method for recording audio and video data using an IC card memory having a mode code region having data for setting recording or playback type of a chapter recorded therein as a recording medium, said method comprising the steps of:

selecting a predetermined chapter;

reading a recording mode address of said selected chapter to determine a mode;

generating a video, an audio or a composite latch out enabling signal in accordance with said determined mode; and

outputting a video, an audio or a composite data in response to said latch out enabling signal.

4. A method for recording audio and video data using an IC card memory as defined in claim 3, further comprising the steps of reading a mode monitoring code in a starting address of said chapter to reconfirm the mode, and proceeding to a next step only when the reconfirmed mode coincides with the determined mode.

5. A method for recording audio and video data, using an IC card, the method comprising:

(i) selecting a recording mode for the selection of audio, video or combined audio/video recording;

(ii) storing mode data on the IC card, the mode data corresponding to the recording mode selected in step (i);

(iii) recording either audio data, video data or combined audio/video data accordingly, on said IC card; and

(iv) storing an address pointer for designating the storage address at which said recording is commenced.

6. A method according to claim 5, the method further comprising any feature or combination of features from the accompanying description, claims, abstract or drawings.

7. An IC card memory substantially as herein described with reference to the accompanying drawings.

8. A method for recording audio and video data substantially as herein described with reference to the accompanying drawings.

The Patent Office

Application No: GB 9606678.2
Claims searched: 1, 2, 5 to 8

Examiner: B G Western
Date of search: 4 July 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G4A AMG1

Int Cl (Ed.6): G06F 12/00 12/02 17/30 ; G11C 7/00

Other: On-line : WPI, Inspec, Computer

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,E	GB-2294562-A	Samsung Electronics Co Limited N.b. pages 21-22, Figures 3, 11, 13	1,5,6,7
X	GB-2248707-A	Fuji Photo Film Co Ltd N.b. pages 6-12	1,5,6,7
A	EP-0220718-A2	Toppan Printing Co Ltd	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.